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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,237	03/19/2004	Yonghua Song	MP0031RE	6605

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,237	SONG, YONGHUA	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-17* is/are allowed.

6)☒ Claim(s) *18-25,29,31-34 and 41-72* is/are rejected.

7)☒ Claim(s) *26-28,30 and 35-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 21 and 37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Limitations "a biasing circuit", "a first bias voltage", "a second bias voltage", and "a third bias voltage" have been recited in claim 20. it is unclear that they are the same. Further, claim 20 recite that the third MOS transistor is in communication with "a second bias voltage", and the "a third bias voltage" is in communication with the second op-amp. It is not seen that "a second bias voltage source to provide a second bias voltage to a second MOS transistor " and "a third bias voltage source to provide a third bias voltage to the third MOS transistor". Therefore, claim 21 is also misdescriptive.

Claim 37 is rejected because there is no antecedent basis for the limitation "the first MOS transistor". Claim 37 should depend on claim 35.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 18-20 and 41-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Des Rosiers et al. (USP 5495184).

As to claim 18, Des Rosiers et al.'s figure 4 shows a temperature and process compensation circuit in communication with control terminals of an active load of an analog integrated circuit to counteract changes in an output level of said analog integrated circuit due to temperature and manufacturing process (intended use), the compensation circuit comprising: a first MOS transistor (N2) having a first source in communication with a common mode voltage (voltage at the source of N2), a first drain, and a first gate in communication with the control terminals (gates of N6, M6, M2); a first differential amplifier (OP1) having a first input in communication with a first bias voltage (VOH), a second input in communication with the first drain, and an output in communication with the control terminals; a second MOS transistor (N4) having a second gate, a second drain in communication with the first drain and a second source; a third MOS transistor (N3) having a third gate in communication with a second bias voltage (Vdac), a third source in communication with a reference point (Vsac), and a third drain in communication with the second source; and a second differential amplifier (OP2) having a second input in communication with the third drain and the second source (via N4), a third input in communication with a third bias voltage (VOL), and an output in communication with the second gate.

As to claim 19, figure 4 shows that the first MOS transistor is of the first conductivity type (P type) and the second and third MOS transistors are of the second conductivity type (N type).

As to claim 20, figure 4 shows a biasing circuit (306, 308, 301, N1) to provide the common mode voltage and to provide the first bias voltage, second bias voltage, and third bias voltage to the compensation circuit.

Claims 41-43 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

3. Claims 22, 23, 25, 29, 32 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagaraj et al. (USP 5642077).

As to claim 22, Nagaraj's figure 1 shows a temperature and process independent analog integrated circuit comprising: analog integrated function means (122, 120, 140, 104) for providing first and second output signals responsive to a first differential input signal and a second differential input; first loading means (124) for providing an output voltage in response to the first output signal, a common mode voltage signal (VCM), and a compensation control signal (at the gate); second loading means (138) for providing an output voltage in response to the second output signal, the common mode voltage signal, and the compensation control signal; and compensation circuit (142, 150) for generating the compensation control signal to compensate for changes due to temperature and manufacturing variations.

As to claim 23, figure 1 shows that the analog integrated function means is selected from the group consisting of multipliers, adaptive filters, function generators, modulators, and neural networks.

As to claim 25, figure 1 shows that the first and second loading means comprise MOS transistors.

As to claim 29, figure 1 shows that biasing means to provide the common mode voltage to the first and second loading means (inherent).

Claims 32 and 34 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Des Rosiers et al. (USP 5495184).

Insofar as understood, Des Rosiers et al.'s figure 4 further shows that the biasing circuit comprising: a common mode voltage source (N1) to provide the common mode voltage; a first bias voltage source (306) to provide the first bias voltage to the first MOS transistor; a second bias voltage source (circuit, not shown, that generates Vdac) to provide the second bias voltage to the second MOS transistor that is referenced to a semiconductor bandgap voltage;and a third bias voltage source (308) to provide a third bias voltage to the third MOS transistor. Thus, figure 4 shows all limitations of the claim except for the voltage sources referenced to a semiconductor bandgap voltage. However, it is notoriously well known in the art that bandgap voltage is independent of temperature. It would have been obvious to one having ordinary to use bandgap voltage source to generate the first to third voltages for the purpose of providing temperature independent voltages.

6. Claims 24 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art figure 3 in view of Nagaraj et al. (USP 5642077).

Applicant's prior art figure 3 shows all limitations of the claim except for the load in communication with a common mode voltage and a compensation circuit. However, Nagaraj's figure 1 shows a circuit having load (124, 138) in communication with compensation circuit (142,

150) and common mode voltage VCM in order to reduce noise. Therefore, it would have been obvious to one having ordinary skill in the art to use Nagaraj's load and compensation circuits for Applicant's prior art's load for the purpose of reducing noise.

7. Claim 31 and 45-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagaraj et al. (USP 5642077).

As to claim 31, Nagaraj's figure 1 fails to teach that the common mode voltage is substantially proportional to a semiconductor bandgap voltage. However, it is notoriously well known in the art that bandgap voltage is temperature independent. Therefore, it would have been obvious to one having ordinary skill in the art to use bandgap voltage to generate the common mode voltage VCM for the purpose providing temperature independent voltage.

As to claim 45, the modified Nagaraj's figure 1 shows an integrated circuits comprising: an analog function circuit (120, 116, 140, 104); a differential loading device (130, 132) in communication with a differential output of the analog function circuit; a compensation circuit (142, 150) in communication with the differential loading device; and a biasing circuit (circuit, not shown, that generates VCM, VDD or bias voltage to the current source 142) in communication with a common mode node of the differential loading device and an input of the compensation circuit, wherein the biasing circuit provides a common mode voltage to the common mode node of the differential loading device and the compensation circuit, and wherein the common mode voltage is independent of temperature and manufacturing process variations (see the rejection of claim 31).

As to claim 46, figure 1 shows that the biasing circuit provides a plurality of control bias voltage signals (VCM, Vdd) to the compensation circuit.

As to claim 47, figure 1 shows that the compensation circuit provides a bias voltage to the differential loading device, and wherein the bias voltage is independent of temperature and manufacturing process variations.

As to claim 48, figure 1 shows that the bias voltage varies a differential loading of the differential loading device.

As to claim 49, figure 1 shows that the bias voltage is comprised of at least the common mode voltage and the plurality of control bias voltage signals (Vdd and bias voltage of the current source 142, figure 3 shows example of current source).

As to claim 50, figure 1 shows that the bias voltage controls a loading on at least one voltage signal associated with the differential loading device.

As to claim 51, figure 1 shows that the differential loading device provides the temperature and process independent output voltage comprised of at least a differential output signal of the analog function circuit, the common mode voltage and the bias voltage.

As to claim 52, figure 1 shows that the plurality of control bias voltage signals are substantially proportional to a semiconductor bandgap voltage (see the rejection of claim 31).

As to claim 53, figure 1 shows that the common mode voltage is substantially proportional to a semiconductor bandgap voltage (see the rejection of claim 31).

As to claim 54, figure 1 shows that the analog function circuit comprises a circuit selected from the group consisting of multipliers, adaptive filters, modulators and neural networks.

As to claim 55, figure 1 shows that the differential loading device comprises first and second transistors (124, 138), wherein the first transistor comprises a first terminal responsive to a first output terminal of the analog function circuit, a second terminal in communication with the common mode node, and a first control terminal; wherein the second transistor comprises a

third terminal responsive to a second output terminal of the analog function circuits a fourth terminal in communication with the common mode node, and a second control terminals and wherein the biasing circuit is in communication with the first and second control terminals.

Claims 56-72 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

Allowable Subject Matter

8. Claims 1-17 are allowed.

9. Claims 26-28, 30 and 35-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-17 are and claims 26-28, 30 and 35-40 would be allowable because the prior art fails to teach or suggest that the compensation circuit comprising the third MOS transistor and differential amplifier connected as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

July 25, 2006